

AC –  
Item No. –

**As Per NEP 2020**

**Tolani College of  
Commerce  
(Autonomous)**



Knowledge is Supreme

**Title of the Course : Digital Electronics**

**Programme: B.Sc(Information System) Semester-II**

**Syllabus for 2 credit Course**

**From the academic year-2024-2025**

Sr. No.	Heading	Particulars
1	<b>Description of the course :</b>	Digital electronics is the study of electronic circuits that are used to process and control digital signals.
2	<b>Vertical :</b>	Minor
3	<b>Type :</b>	Theory and Practical
4	<b>Credit:</b>	2 credits (1 Credit = Theory and 1 Credit = Project Work)
5	<b>Hours Allotted :</b>	30 Hours
6	<b>Marks Allotted:</b>	50 Marks Continuous Evaluation =20 Semester End =30
7	<b>Course Objectives:</b>	<ol style="list-style-type: none"> <li>1. To understand the importance of various number system used in digital circuit, along with Boolean equations related to digital circuit.</li> <li>2. To understand the role of K map in designing combinational circuits.</li> </ol>
8	<b>Course Outcomes:</b>	<ol style="list-style-type: none"> <li>1. Students will be able to understand and examine the structure of various number systems and its storage and application in computer system.</li> <li>2. Students will be able to understand, analyses and design various combinational circuits.</li> </ol>

<b>9</b>	<p><b>Module 1: Number System, Binary Arithmetic, Boolean Algebra and Logic Gates (15 Hours)</b></p> <ul style="list-style-type: none"> <li>Binary number system, octal number system, hexadecimal number system, conversion from one number system to another, weighted codes binary coded decimal, non-weighted codes Excess – 3 code, Gray code</li> <li>Binary addition, Binary subtraction, Negative number representation, Subtraction using 1's complement and 2's complement, Binary multiplication and division, Arithmetic in octal number system</li> <li>Introduction, Logic (AND OR NOT), Boolean theorems, Boolean Laws, De Morgan's Theorem, Perfect Induction, Reduction of Logic expression using Boolean Algebra, Deriving Boolean expression from given circuit, exclusive OR and Exclusive NOR gates, Universal Logic gates, Implementation of other gates using universal gates</li> </ul> <p><b>Module 2: Minterm, Maxterm Karnaugh Maps, Combinational Logic Circuits, Multiplexer, Demultiplexer, ALU, Encoder and Decoder (15 Hours)</b></p> <ul style="list-style-type: none"> <li>Introduction, minterms and sum of minterm form, maxterm and Product of maxterm form, Reduction technique using Karnaugh maps – 2/3/4 variable K-maps, Grouping of variables in K-maps, K-maps for product of sum form, minimize Boolean expression using K-map and obtain K-map from Boolean expression.</li> <li>Introduction, Multi-input, multi-output Combinational circuits, Codeconverters design and implementations, Multiplexer, Demultiplexer, Decoder, ALU, Encoders</li> <li>Introduction, Terminologies used, S-R flip-flop, D flip-flop, JK flip-flop, Race-around condition, Master – slave JK flip-flop, T flip-flop</li> </ul>
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<b>11</b>	<p><b>Reference Books:</b></p> <ul style="list-style-type: none"> <li><b>Author: R.P Jain Title :</b> Modern Digital Electronics <b>Publisher:</b> Mc Graw Hill, 5<sup>th</sup> Edition, <b>Year:</b> 2022</li> <li><a href="https://e-next.in/bsc-it/sem1/digital-electronics/">https://e-next.in/bsc-it/sem1/digital-electronics/</a></li> </ul>											
<b>12</b>	<b>Internal Continuous Assessment: 20%</b>	<b>Semester End Examination : 30%</b>										
<b>13</b>	<b>Continuous Evaluation through:</b>	Practical Assessment										
<b>14</b>	<p><b>Format of Question Paper:</b></p> <p style="text-align: center;"><b>Scheme of Evaluation Pattern</b>  <b>Table 1A: Scheme of Continuous Evaluation (CE/Practical)</b>  <b>Scheme of Evaluation Pattern</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">Sub-components</th> <th style="text-align: center;">Maximum Marks</th> <th style="text-align: center;">Conditions for passing</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1) Practical exam</td> <td style="text-align: center;">15</td> <td rowspan="3" style="text-align: center; vertical-align: middle;">A learner must be present for each of the sub-components.</td> </tr> <tr> <td style="text-align: center;">2) Journal and Viva</td> <td style="text-align: center;">5</td> </tr> <tr> <td style="text-align: center;">Total</td> <td style="text-align: center;">20</td> </tr> </tbody> </table>		Sub-components	Maximum Marks	Conditions for passing	1) Practical exam	15	A learner must be present for each of the sub-components.	2) Journal and Viva	5	Total	20
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1) Practical exam	15	A learner must be present for each of the sub-components.										
2) Journal and Viva	5											
Total	20											

**Table 1B: Scheme of Semester End Examination (SEE) Evaluation  
Question Paper Pattern for Semester End Examination (SEE)**

**Maximum Marks: 30**

**Duration: I Hrs.**

Note: All questions are compulsory. Each question has an internal choice.

Question Number	Nature of Questions	Maximum Marks
1)	<b>Attempt any 3</b>	
	a)	15
	b)	
	c)	
	d)	
	e)	
2)	<b>Attempt any 3</b>	
	a)	15
	b)	
	c)	
	d)	
	e)	